| REVISIONS | | | |
|---|---|---|---|
| LTR | DESCRIPTION | DATE | APPROVED |
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Prepared in accordance with ASME Y14.24

Vendor item drawing

| | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **REV** | | | | | | | | | | | | | | | | | | | | | |
| **PAGE** | | | | | | | | | | | | | | | | | | | | | |
| **REV** | | | | | | | | | | | | | | | | | | | | | |
| **PAGE** | | | | | | | | | | | | | | | | | | | | | |
| **REV STATUS OF PAGES** | **REV** | | | | | | | | | | | | | | | | | | | | |
| | **PAGE** | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | | | | | | | |

| | | |
|---|---|---|
| **PMIC N/A** | **PREPARED BY**<br>RICK OFFICER | **DEFENSE SUPPLY CENTER, COLUMBUS**<br>**COLUMBUS, OHIO** |
| Original date of drawing<br>YY MM DD<br>04-04-19 | **CHECKED BY**<br>TOM HESS | **TITLE**<br>MICROCIRCUIT, DIGITAL, HEX INVERTER, MONOLITHIC SILICON |
| | **APPROVED BY**<br>RAYMOND MONNIN | |
| | **SIZE** A / **CODE IDENT. NO.** 16236 | **DWG NO.** V62/04691 |
| | **REV** | **PAGE** 1 **OF** 13 |

AMSC N/A

5962-V091-04

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance hex inverter microcircuit, with an operating temperature range of -40°C to +105°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturers PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

| V62/04691 | - | 01 | X | E |
|---|---|---|---|---|
| Drawing number | | Device type (See 1.2.1) | Case outline (See 1.2.2) | Lead finish (See 1.2.3) |

1.2.1 Device type(s).

| Device type | Generic | Circuit function |
|---|---|---|
| 01 | SN74LV04A-EP | Hex inverter |

1.2.2 Case outline(s). The case outlines shall be as specified herein.

| Outline letter | Number of pins | JEDEC PUB 95 | Package style |
|---|---|---|---|
| X | 14 | MO-153 | Plastic small outline |

1.2.3 Lead finishes. The lead finishes shall be as specified below or other lead finishes as provided by the device manufacture:

| Finish designator | Material |
|---|---|
| A | Hot solder dip |
| B | Tin-lead plate |
| C | Gold plate |
| D | Palladium |
| E | Gold flash palladium |
| Z | Other |

1.3 Absolute maximum ratings. 1/

Supply voltage range ( $V_{CC}$ ) ..... -0.5 V to 7 V
Input voltage range ( $V_I$ ) ..... -0.5 V to 7 V 2/
Voltage range applied to any output in the high impedance or power off state ( $V_O$ ) ..... -0.5 V to 7 V 2/
Output voltage range ( $V_O$ ) ..... -0.5 V to $V_{CC}$ +0.5 V 2/ 3/
Input clamp current ( $I_{IK}$ ) ( $V_I < 0$ ) ..... -20 mA
Output clamp current ( $I_{OK}$ ) ( $V_O <$ 0 or $V_O > V_{CC}$ ) ..... ±50 mA
Continuous output current ( $I_O$ ) ( $V_O$ = 0 to $V_{CC}$ ) ..... ±25 mA
Continuous current through $V_{CC}$ or GND ..... ±50 mA
Package thermal impedance ( $\theta_{JA}$ ) ..... 113°C/W 4/
Storage temperature range ($T_{STG}$) ..... -65°C to 150°C

1.4 Recommended operating conditions. 5/ 6/

Supply voltage range ( $V_{CC}$ ) ..... 2 V minimum to 5.5 V maximum
High level input voltage ( $V_{IH}$ ):
$V_{CC}$ = 2 V ..... 1.5 V minimum
$V_{CC}$ = 2.3 V to 2.7 V ..... $V_{CC}$ x 0.7 V minimum
$V_{CC}$ = 3 V to 3.6 V ..... $V_{CC}$ x 0.7 V minimum
$V_{CC}$ = 4.5 V to 5.5 V ..... $V_{CC}$ x 0.7 V minimum
Low level input voltage ( $V_{IL}$ ):
$V_{CC}$ = 2 V ..... 0.5 V maximum
$V_{CC}$ = 2.3 V to 2.7 V ..... $V_{CC}$ x 0.3 V maximum
$V_{CC}$ = 3 V to 3.6 V ..... $V_{CC}$ x 0.3 V maximum
$V_{CC}$ = 4.5 V to 5.5 V ..... $V_{CC}$ x 0.3 V maximum
Input voltage ( $V_I$ ) ..... 0 V minimum to 5.5 V maximum
Output voltage ( $V_O$ ) ..... 0 V minimum to $V_{CC}$ maximum
High level output current ( $I_{OH}$ ):
$V_{CC}$ = 2 V ..... -50 µA maximum
$V_{CC}$ = 2.3 V to 2.7 V ..... -2 mA maximum
$V_{CC}$ = 3 V to 3.6 V ..... -6 mA maximum
$V_{CC}$ = 4.5 V to 5.5 V ..... -12 mA maximum

---

1/ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2/ The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
3/ This value is limited to 5.5 V maximum.
4/ The package thermal impedance is calculated in accordance with JESD 51-7.
5/ All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation.
6/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

1.4 Recommended operating conditions - continued. 5/ 6/

Low level output current ( $I_{OL}$ ):
- $V_{CC}$ = 2 V ..... 50 µA maximum
- $V_{CC}$ = 2.3 V to 2.7 V ..... 2 mA maximum
- $V_{CC}$ = 3 V to 3.6 V ..... 6 mA maximum
- $V_{CC}$ = 4.5 V to 5.5 V ..... 12 mA maximum

Input transition rise or fall rate ( $\Delta t / \Delta v$ ):
- $V_{CC}$ = 2.3 V to 2.7 V ..... 200 ns / V maximum
- $V_{CC}$ = 3 V to 3.6 V ..... 100 ns / V maximum
- $V_{CC}$ = 4.5 V to 5.5 V ..... 20 ns / V maximum

Operating free-air temperature range ( $T_A$ ) ..... -40°C to +105°C

2. APPLICABLE DOCUMENTS

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Applications for copies should be addressed to the Electronic Industry Alliance, 2500 Wilson Boulevard, Arlington, VA 22201-3834 or at http://www.jedec.org)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Truth table. The truth table shall be as shown in figure 3.

3.5.4 Logic diagram. The logic diagram shall be as shown in figure 4.

3.5.5 Timing waveforms and test circuit. The timing waveforms and test circuit shall be as shown in figure 5.

TABLE I. Electrical performance characteristics.

| Test | Symbol | Conditions | Temperature, $T_A$ | Device type | Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| Electrical characteristics section. | | | | | | | |
| High level output voltage | $V_{OH}$ | $I_{OH}$ = -50 µA, $V_{CC}$ = 2 V to 5.5 V | -40°C to 105°C | 01 | $V_{CC}$ – 0.1 | | V |
| | | $I_{OH}$ = -2 mA, $V_{CC}$ = 2.3 V | | | 2 | | |
| | | $I_{OH}$ = -6 mA, $V_{CC}$ = 3 V | | | 2.48 | | |
| | | $I_{OH}$ = -12 mA, $V_{CC}$ = 4.5 V | | | 3.8 | | |
| Low level output voltage | $V_{OL}$ | $I_{OL}$ = 50 µA, $V_{CC}$ = 2 V to 5.5 V | -40°C to 105°C | 01 | | 0.1 | V |
| | | $I_{OL}$ = 2 mA, $V_{CC}$ = 2.3 V | | | | 0.4 | |
| | | $I_{OL}$ = 6 mA, $V_{CC}$ = 3 V | | | | 0.44 | |
| | | $I_{OL}$ = 12 mA, $V_{CC}$ = 4.5 V | | | | 0.55 | |
| Input current | $I_I$ | $V_I$ = 5.5 V or GND, $V_{CC}$ = 0 to 5.5 V | -40°C to 105°C | 01 | | ±1 | µA |
| Supply current | $I_{CC}$ | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0, $V_{CC}$ = 5.5 V | -40°C to 105°C | 01 | | 20 | µA |
| Off current | $I_{off}$ | $V_I$ or $V_O$ = 0 to 5.5 V, $V_{CC}$ = 0 | -40°C to 105°C | 01 | | 5 | µA |
| Input capacitance | $C_i$ | $V_I$ = $V_{CC}$ or GND, $V_{CC}$ = 3.3 V | -40°C to 105°C | 01 | 2.3 typical | | pF |
| | | $V_I$ = $V_{CC}$ or GND, $V_{CC}$ = 5 V | | | 2.3 typical | | |
| Switching characteristics section. See figure 5 | | | | | | | |
| Power dissipation time | $t_{pd}$ | From input A, to output Y, | +25°C | 01 | | 15.5 | ns |
| | | $V_{CC}$ = 2.5 V ±0.2 V, $C_L$ = 50 pF | -40°C to 105°C | | 1 | 18 | |
| | | From input A, to output Y, | +25°C | | | 10.6 | |
| | | $V_{CC}$ = 3.3 V ±0.3 V, $C_L$ = 50 pF | -40°C to 105°C | | 1 | 12 | |
| | | From input A, to output Y, | +25°C | | | 7.5 | |
| | | $V_{CC}$ = 5 V ±0.5 V, $C_L$ = 50 pF | -40°C to 105°C | | 1 | 8.5 | |

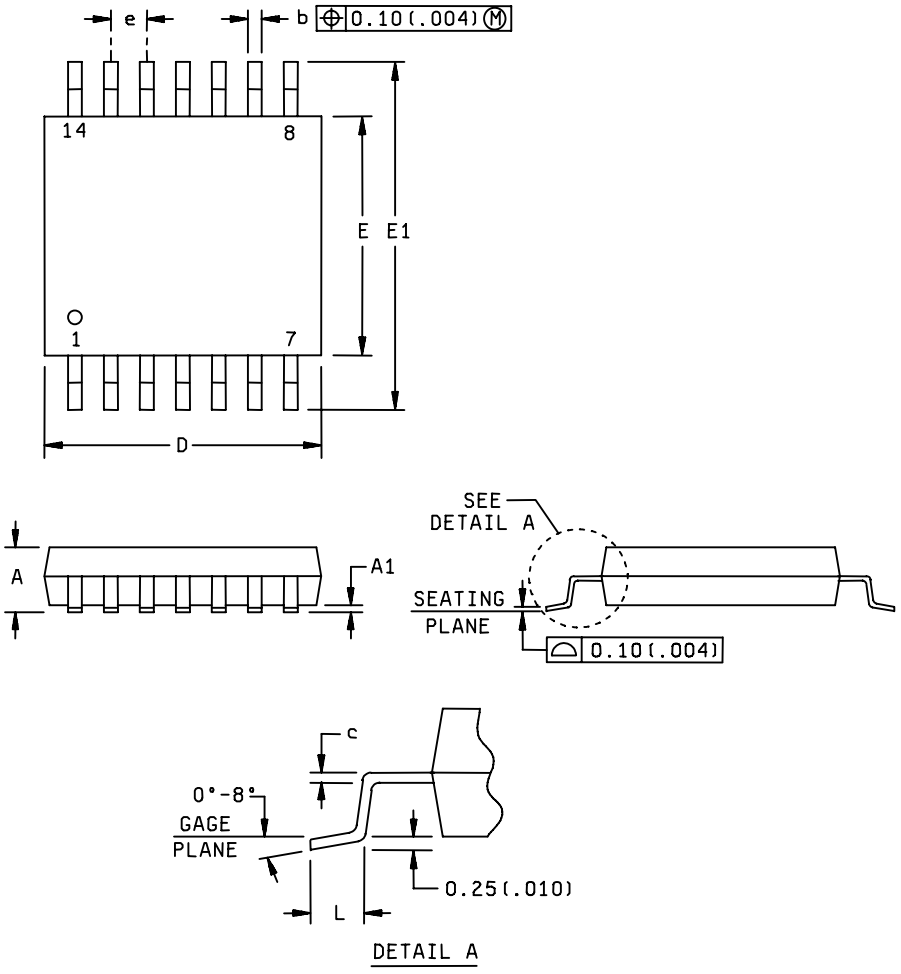
See footnotes at end of table.

TABLE I. Electrical performance characteristics – continued.

| Test | Symbol | Conditions | Temperature, $T_A$ | Device type | Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| Noise characteristics section. | | 1/ | | | | | |
| Quiet output, maximum dynamic $V_{OL}$ | $V_{OL(P)}$ | $V_{CC}$ = 3.3 V, $C_L$ = 50 pF | +25°C | 01 | | 0.8 | V |
| Quiet output, minimum dynamic $V_{OL}$ | $V_{OL(V)}$ | $V_{CC}$ = 3.3 V, $C_L$ = 50 pF | +25°C | 01 | | -0.8 | V |
| Quiet output, minimum dynamic $V_{OH}$ | $V_{OH(V)}$ | $V_{CC}$ = 3.3 V, $C_L$ = 50 pF | +25°C | 01 | 3.1 typical | | V |
| High level dynamic input voltage | $V_{IH(D)}$ | $V_{CC}$ = 3.3 V, $C_L$ = 50 pF | +25°C | 01 | 2.31 | | V |
| Low level dynamic input voltage | $V_{IL(D)}$ | $V_{CC}$ = 3.3 V, $C_L$ = 50 pF | +25°C | 01 | | 0.99 | V |
| Operating characteristics section. | | | | | | | |
| Power dissipation capacitance | $C_{pd}$ | $V_{CC}$ = 3.3 V, $C_L$ = 50 pF, f = 10 MHz | +25°C | 01 | 9.6 typical | | pF |
| | | $V_{CC}$ = 5 V, $C_L$ = 50 pF, f = 10 MHz | | | 11.4 typical | | |

1/ Characteristics are for surface mount packages only.

Case X




NOTES:
1. This drawing is subject to change without notice.
2. Body dimensions do not include mold flash or protrusion not to exceed 0.15 mm (0.006 inches).
3. Falls within JEDEC MO-153.
4. All linear dimensions are shown in millimeters (inches). Inches equivalents are given for general information only.

FIGURE 1. Case outline.

Case X

| Symbol | Dimensions | | | |
|---|---|---|---|---|
| | Millimeters | | Inches | |
| | Min | Max | Min | Max |
| A | | 1.20 | | 0.047 |
| A1 | 0.05 | 0.15 | 0.002 | 0.006 |
| b | 0.19 | 0.30 | 0.007 | 0.012 |
| c | 0.15 NOM | | 0.006 NOM | |
| D | 4.90 | 5.10 | 0.193 | 0.201 |
| E | 4.30 | 4.50 | 0.169 | 0.177 |
| E1 | 6.20 | 6.60 | 0.244 | 0.260 |
| e | 0.65 NOM | | 0.026 NOM | |
| L | 0.50 | 0.75 | 0.020 | 0.030 |

FIGURE 1. Case outline - Continued.

| Device type | 01 |
|---|---|
| Case outline | X |
| Terminal number | Terminal symbol |
| 1 | 1A |
| 2 | 1Y |
| 3 | 2A |
| 4 | 2Y |
| 5 | 3A |
| 6 | 3Y |
| 7 | GND |
| 8 | 4Y |
| 9 | 4A |
| 10 | 5Y |
| 11 | 5A |
| 12 | 6Y |
| 13 | 6A |
| 14 | $V_{CC}$ |

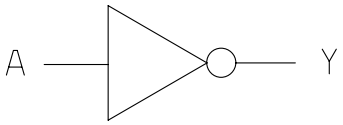
FIGURE 2. Terminal connections.

( Each inverter )

| Input | Output |
|---|---|
| A | Y |
| H | L |
| L | H |

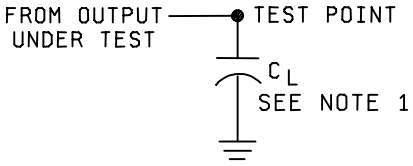
H = High voltage level
L = Low voltage level
X = Don’t care

FIGURE 3. Truth table.

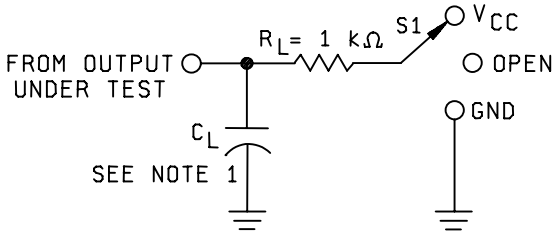



Each inverter (positive logic)

FIGURE 4. Logic diagram.



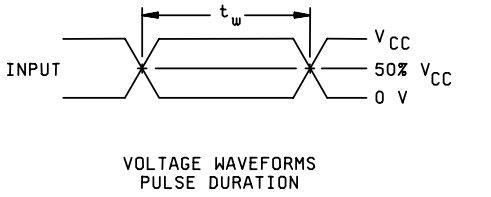

LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS



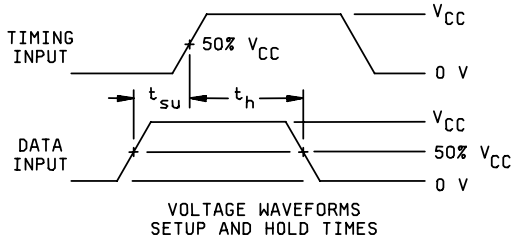

LOAD CIRCUIT FOR
3-STATE AND OPEN-DRAIN OUTPUTS

| Test | S1 |
|---|---|
| $t_{PLH}$ / $t_{PHL}$ | Open |
| $t_{PLZ}$ / $t_{PZL}$ | $V_{CC}$ |
| $t_{PHZ}$ / $t_{PZH}$ | GND |
| Open drain | $V_{CC}$ |

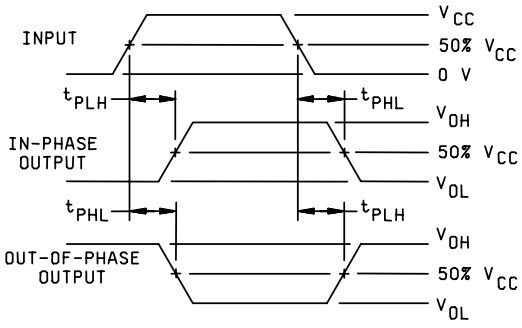
FIGURE 5. Timing waveforms and test circuit.



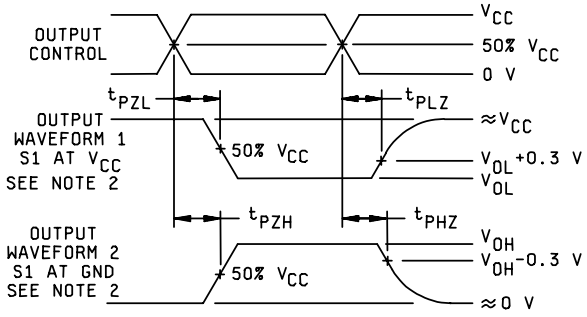

VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW AND HIGH-LEVEL ENABLING

NOTES:

1. $C_L$ includes probe and jig capacitance.
2. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
   Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
3. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 3 ns, and $t_f$ ≤ 3 ns.
4. The outputs are measured one at a time with one input transition per measurement.
5. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
6. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
7. $t_{PHL}$ and $t_{PLH}$ are the same as $t_{pd}$.
8. All parameters and waveforms are not applicable to all devices.

FIGURE 5. Timing waveforms and test circuit – Continued.

4.0 QUALITY ASSURANCE PROVISIONS

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5.0 PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6.0 NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item.

| Vendor item drawing administrative control number 1/ | Device manufacturer CAGE code | Package | | Vendor part number | Top side marking |
|---|---|---|---|---|---|
| V62/04691-01XE | 01295 | TSSOP - PW | Tape and reel | SN74LV04ATPWREP | LV04AEP |

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

| CAGE code | Source of supply |
|---|---|
| 01295 | Texas Instruments, Inc.<br>Semiconductor Group<br>8505 Forest lane<br>P.O. Box 660199<br>Dallas, TX 75243<br>Point of contact: U.S. Highway 75 South<br>P.O. Box 84, M/S 853<br>Sherman, TX 75090-9493 |